Abstract of the Disclosure

In a prefetch-type FCRAM having an improved data write control circuit and a method of masking data using the prefetch-type FCRAM, the prefetch-type FCRAM includes a command decoder, a row decoder, a column decoder, a data input buffer, a data output buffer, and a valid write window buffer. The command decoder outputs control commands including first and second write commands in response to predetermined external input signals. The row decoder decodes a row address signal input into the address pins and activates a wordline of the memory cell array corresponding to the decoded row address signal. The column decoder decodes a column address signal input into the address pins and activates a column select line of the memory cell array corresponding to the decoded column address signal. The data input buffer receives input data from the plurality of data pins and then outputs the input data in synchronization with a predetermined clock signal. The data output buffer outputs output data read from the memory cell array to the plurality of data pins. The valid write window buffer outputs a data masking control signal that controls the masking of input data in response to a combined address signal input into the address pins.

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